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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/783,821	02/14/2001	Carl H. Carmichael	X-722 US	2727

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/783,821	CARMICHAEL ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-35* is/are allowed.

6)☒ Claim(s) *23-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 23-35 are presented for examination. Claims 1-22 and 36-48 have been cancelled.

Election/Restrictions

Applicant's election without traverse of Group III, claims 23-35 in the reply filed on July 19, 2004 is acknowledged.

Drawings

The drawings were received on February 14, 2001. These drawings are acceptable.

Allowable Subject Matter

Claims 33-35 are allowable over the prior arts of record.

These claims recite such features as a method of correcting an expected error in configuration data by determining the frequency of the expected error and reconfiguring the configuration data with a scrub frequency based on the determined error frequency without determining whether an error has occurred.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 30-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Schultz et al. U. S. Patent No. 6,191,614.

As per claim 30, Schultz et al. teach the claimed method in which FPGA configuration data circuitry is connected with a CRC circuit in order to identify configuration data errors. When the error is detected, partial reconfiguration capability is used to reconfigure only the portion in error. (Column 2 lines 39-56, column 2 lines 27-36)

As per claims 31 and 32, a frame mask register is provided in the configuration memory that controls which memory cells of each frame (column) are written during a configuration operation, thereby allowing selective access to individual groups of configuration data stored in the memory array. Thereby requiring limited readback and using the CRC data. (Column 3 lines38-43, column 4 lines 61-65)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 23- 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alfke U.S. Patent No. 6,104,211 in view of Kwait U.S. Patent No. 5,931,959.

As per claim 23, Alfke substantially teaches the claimed method in which PLDs are in parallel to provide identical logic functions. To guard against data corruption that can result from radiation-induced upsets, the logic circuit includes a state-comparison

circuit that periodically performs a bitwise comparison of the configuration and user data from each of the PLDs; if a bit from one PLD differs from the corresponding bit from the others, the state-comparison circuit sets a flag that indicates that the differing PLD is in error. (Abstract) Not disclosed by Alfke is that the comparison is preformed on the checksum generated by the device.

However, in an analogous art, Kwait teaches using checksum and/or CRC to send to a comparison output from the FPGA circuit (column 10 lines 10-22 and 45-55 figures 10 and 11). Therefore, it would have been obvious to one of ordinary skill in the art at the time this invention was made to have used a computed error correction code in the comparison steps of the circuit of Alfke. This would have been obvious as suggested by Kwait combating some faults requires more complex algorithmic or heuristic approaches that check whether outputs meet user-defined reasonableness criteria. (Abstract)

As per claim 24, Alfke teaches reconfiguration of PLDs which receive the error flag (figure 3, column 2 lines 30-38).

As per claim 25, Alfke teaches the use of a configurable logic module as a control function for the PLD (column 3 lines 1-10).

As per claim 26, Alfke teaches identically configured PLDs in parallel and the configurable logic includes a comparison circuit (column 2 lines 60-64).

As per claim 27, Alfke substantially teaches the claimed method in which PLDs are in parallel to provide identical logic functions. To guard against data corruption that can result from radiation-induced upsets, the logic circuit includes a state-comparison

circuit that periodically performs a bitwise comparison of the configuration and user data from each of the PLDs; if a bit from one PLD differs from the corresponding bit from the others, the state-comparison circuit sets a flag that indicates that the differing PLD is in error. (Abstract, column 5 lines 7-14) Not disclosed by Alfke is that the comparison is preformed on the checksum generated by the device.

However, in an analogous art, Kwait teaches using checksum and/or CRC to send to a comparison output from the FPGA circuit (column 10 lines 10-22 and 45-55 figures 10 and 11). Therefore, it would have been obvious to one of ordinary skill in the art at the time this invention was made to have used a computed error correction code in the comparison steps of the circuit of Alfke. This would have been obvious as suggested by Kwait combating some faults requires more complex algorithmic or heuristic approaches that check whether outputs meet user-defined reasonableness criteria. (Abstract)

As per claim 28, Alfke teaches reconfiguration of PLDs that receive the error flag (figure 3, column 2 lines 30-38).

As per claim 29, Alfke teaches the use of a configurable logic module as a control function for the PLD (column 3 lines 1-10).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Publication 2001/0032318 Yip et al.

This patent teaches a method an apparatus for protecting a configuration data sequence from reverse engineering. The configuration data sequence includes a plurality of configuration bits and is used to configure the operation of a programmable device, such as an FPGA or other reconfigurable logic. According to a method of the present invention, the configuration bits of the configuration data sequence are partially encrypted by altering some, but not all, of the bits, and subsequently storing the partially-encrypted configuration data sequence external to the programmable device. Corresponding decryption information is then stored within the programmable device, which decrypts the partially-encrypted configuration data sequence using the decryption information stored therein to thereby configure internal logic of the programmable device.

U.S. Patent Nos. 6,560,743 and 6,237,124 Plants, William C.

These patents teach methods for detecting an error in data stored in configuration SRAM and user assignable SRAM in a FPGA comprises the steps of providing a serial data stream into the FPGA from an external source, loading data from the serial data stream into the configuration SRAM in response to address signals generated by row column counters, loading data from the serial data stream into the user assignable SRAM in response to address signals generated by row and column counters, loading a seed and signature from the serial data stream into a cyclic redundancy checking circuit, cycling data out of the configuration SRAM and the user

assignable SRAM by the row and column counters; performing error checking on the data that has been cycled out of the configuration SRAM and out of the user assignable SRAM by the cyclic redundancy checking circuit, and generating an error signal when an error is detected by the error checking circuit.

U.S. Patent No. 6,526,559 Schiefele et al.

This patent teaches a field programmable gate array (FPGA) allowing dynamic reconfiguration in time multiplexing fashion; duplicate copies are configured in a time multiplexing manner which are functionally identical to a primary circuit specified for a predetermined FPGA's application. The primary and duplicate circuits are interrogated by a voting circuit, which determines the existence of a faulted circuit in order to eliminate the faulted circuit from the operation of the FPGA. In this manner, without physical addition of redundant circuits, fault tolerancy for the FPGA is provided to minimize the cost, weight, volume, heat and energy associated issues of conventional redundancy techniques.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

GUY LAMARRE
PRIMARY EXAMINER